AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Currently amended) A method of forming a static random access memory device contact stud with an integral resistor, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. forming the integral resistor by disposing a thin resistive ~~material~~ film layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

wherein said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said static random access memory device, the thin resistive film ~~material~~ layer located in a cross coupling between an M1 metal cross coupling node and a polysilicon gate node at either a contact-to-M1 interface or a contact-to-polysilicon gate interface;

further comprising the step of limiting a width of the thin resistive film ~~material~~ layer to a width of the contact hole.

4. (Currently amended) A method of forming a bipolar transistor contact stud with an integral resistor, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. forming the integral resistor by disposing a resistive material layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

wherein said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said bipolar transistor, the integral resistor has a resistance value of between about one Ohm and about ten Ohms, and the integral resistor is in circuit series connection with said contact stud with a base, emitter or collector of the bipolar transistor.

5. (Original) The method of claim 4, wherein the bipolar transistor is a silicon-on-insulator lateral diode, and the integral resistor and contact stud form a local resistor element in at least one of an anode, a cathode or a gate.

6. (Original) The method of claim 4, further comprising the step of placing a gate structure in parallel circuit connections to the local resistor element.

7. (Currently amended) A method of forming an integral resistor and contact stud within a contact hole within a semiconductor transistor drain structure, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area;

e. forming the integral resistor by disposing a resistive material layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

f. placing the integral resistor and contact stud in a circuit series connection with a gate, the resistor having a resistance value of between about one Ohm and about ten Ohms, wherein the drain has a composite resistance not equal to a source composite

resistance and said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said semiconductor.

8. (Original) The method of claim 7 wherein the device is a MOSFET and the integral resistor and contact stud form a first local resistor, further comprising the steps of:

forming a second integral resistor and contact stud within a contact hole within a gate, the second integral resistor having a resistance greater than about 10 Ohms;

placing the second integral resistor and second contact stud in a circuit series connection with the first local resistor.

9. (Original) The method of claim 8, further comprising the step of coupling the gate to ground through the second integral resistor.

10. (Previously presented) The method of claim 7, wherein the device is a MOSFET, further comprising the step of modulating current flow through the MOSFET by selective placement of a plurality of integral resistor and contact stud structures throughout the drain.

11. (Original) The method of claim 10 wherein the step of modulating current flow comprises the step of forming a plurality of contacts on a drain side of the MOSFET;

wherein the step of forming the integral resistor and contact stud comprises forming an integral resistor and a contact stud structure within each of a group of the plurality of contacts in an interdigitated pattern, the pattern comprising an alternating distribution of contacts and integral resistor and contact stud structures.

12. (Previously presented) A method of forming a SiGe transistor contact stud with an integral resistor, said method comprising the steps of:

a. providing a substrate having at least one contact area;

b. forming an insulating layer over said substrate, said insulating layer overlying and in contact with the contact area;

c. forming a contact hole in a base region or above an emitter in said insulating layer to expose the contact area;

d. providing a first conductive material into the contact hole to form a contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. forming the integral resistor by disposing a resistive material layer within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface;

wherein said integral resistor is in a circuit series connection with said contact stud between the contact area and an electrical node of said SiGe transistor, and

modulating current flow through the transistor by selective placement of a plurality of the integral resistor and contact stud structures throughout the base region or

above the emitter, thereby changing the effective base resistance when the plurality of integral resistor and contact stud structures are located in the base region.

13. (Original) The method of claim 12 wherein the integral resistor has a resistance value of from about one to about ten Ohms.

14. (Original) The method of claim 12 wherein the step of modulating current flow comprises the step of forming a plurality of contacts in the base region;

wherein the step of forming the integral resistor and contact stud comprises forming an integral resistor and a contact stud structure within each of a group of the plurality of contacts in an interdigitated pattern, the pattern comprising an alternating distribution of contacts and integral resistor and contact stud structures.

15. (Canceled)

16. (Canceled)

17. (Currently amended) The method of claim 12 wherein the step of modulating current flow comprises the step of selectively ~~placeing~~ placing a plurality of integral resistor and contact stud structures above the emitter.

18. (Currently amended) ~~he~~ The method of claim 17 wherein the step of modulating current flow comprises the step of forming a plurality of contacts above the emitter;

wherein the step of forming the integral resistor and contact stud comprises forming an integral resistor and a contact stud structure within each of a group of the plurality of contacts in an interdigitated pattern, the pattern comprising an alternating distribution of contacts and integral resistor and contact stud structures.

19. (Previously presented) A method for integrating a local resistor element with a semiconductor device contact, the local resistor element having a resistance value of from about one Ohm to about 100 Ohms, comprising the following steps:

forming a contact on an interlevel dielectric;

depositing a first thin resistor film on said interlevel dielectric and said contact;

masking said contact where the local resistor is to be formed;

etching to remove the first resistor thin film;

depositing a refractory metal film;

depositing a conductive metal; and

polishing said interlevel dielectric surface.

20. (Original) The method of claim 19, further comprising the following steps prior to the masking step:

oxidizing the first thin resistor film;

depositing a second thin resistor film on the first thin resistor film; and

oxidizing the second thin resistor film.

21. (Canceled)

22. (Canceled)

23. (Currently amended) A static random access memory device having a contact stud with an integral resistor, comprising:

a. a substrate having at least one contact area;

b. an insulating layer formed over said substrate, said insulating layer overlying and in contact with the contact area;

c. a contact hole formed in said insulating layer to expose the contact area;

d. a contact stud disposed in the contact hole, said contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. ~~an~~ a thin integral resistive ~~material~~ film layer disposed within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface, wherein said thin resistive film layer and said contact stud form a local resistor structure; wherein said local resistor structure is in a circuit series connection between the contact area and an electrical node of said static random access memory device, and the thin resistive ~~material~~ film layer is located in a cross coupling between an M1 metal cross coupling node and a polysilicon gate node at either a contact-to-M1 interface or a contact-to-polysilicon gate interface; and

wherein the thin resistive film layer ~~material~~ further has a width no greater than the width of the contact hole.

24. (Previously presented) A bipolar transistor having a contact stud with an integral resistor, comprising:

a. a substrate having at least one contact area;

b. an insulating layer formed over said substrate, said insulating layer overlying and in contact with the contact area;

c. a contact hole formed in said insulating layer to expose the contact area;

d. a contact stud disposed in the contact hole, said contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. an integral resistive material layer disposed within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface, wherein said resistive layer and said contact stud form a local resistor structure;

wherein said local resistor structure is in a circuit series connection between the contact area and an electrical node of said bipolar transistor, the integral resistor has a resistance value of between about one Ohm and about ten Ohms, and the integral resistor is in circuit series connection with said contact stud with a base, emitter or collector of the bipolar transistor.

25. (Original) The semiconductor device of claim 24, wherein the bipolar transistor is a silicon-on-insulator lateral diode, and the integral resistor and contact stud form a local resistor element in at least one of an anode, a cathode or a gate.

26. (Original) The semiconductor device of claim 24, wherein a gate structure is in parallel circuit connection to the local resistor element.

27. (Previously presented) A semiconductor device having a contact stud with an integral resistor, comprising:

a. a substrate having at least one contact area;

b. an insulating layer formed over said substrate, said insulating layer overlying and in contact with the contact area;

c. a contact hole formed in said insulating layer to expose the contact area;

d. a contact stud disposed in the contact hole, said contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. an integral resistive material layer disposed within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface, wherein said resistive layer and said contact stud form a local resistor structure;

wherein said local resistor structure is in a circuit series connection between the contact area and an electrical node of said semiconductor device,

wherein the local resistor structure and contact hole are formed within a transistor drain structure, the local resistor structure in a circuit series connection with a gate, the resistor having a resistance value of between about one Ohm and about ten Ohms,

and wherein the drain has a composite resistance not equal to a source resistance.

28. (Original) The semiconductor device of claim 27 wherein the device is a MOSFET and the local resistor structure forms a first local resistor, further comprising:

a second integral resistor disposed on a second stud within a contact hole within a gate, the second integral resistor having a resistance greater than about 10 Ohms; and

the second integral resistor and second contact stud further in a circuit series connection with the first local resistor.

29. (Original) The semiconductor device of claim 28, wherein the gate is coupled to ground through the second integral resistor.

30. (Previously presented) The semiconductor device of claim 27 wherein the device is a MOSFET, further comprising a plurality of integral resistor and contact stud structures, in which a placement of the plurality of integral resistor and contact stud structures relative to other contact structures placed within the drain modulates current flow through the MOSFET.

31. (Original) The semiconductor device of claim 30, wherein a plurality of local resistor structures are located within the drain in an interdigitated pattern relative to the other contact structures, the pattern comprising an alternating distribution of other contacts and local resistor structures.

32. (Previously presented) A SiGe transistor having a contact stud with an integral resistor, comprising:

a. a substrate having at least one contact area;

b. an insulating layer formed over said substrate, said insulating layer overlying and in contact with the contact area;

c. a contact hole formed in said insulating layer to expose the contact area, the contact hole in a base region or above an emitter:

d. a contact stud disposed in the contact hole, said contact stud having an upper surface and a lower surface, the lower surface in circuit connection with the contact area; and

e. an integral resistive material layer disposed within the contact hole on at least one of the contact stud upper surface and the contact stud lower surface, wherein said resistive layer and said contact stud form a local resistor structure;

wherein said local resistor structure is in a circuit series connection between the contact area and an electrical node of said SiGe transistor,

wherein the placement of a plurality of integral resistor and contact stud structures relative to other contact structures placed within the base region or above the emitter modulates current flow through the transistor, wherein if the local resistor structure contact hole is in the base region then thereby changing an effective base resistance.

33. (Original) The semiconductor device of claim 32, wherein the integral resistor has a resistance value of from about one to about ten Ohms.

34. (Previously presented) The semiconductor device of claim 33, wherein the local resistor structure contact hole is in the base region , further comprising a plurality of

local resistor structures located within the base region in an interdigitated pattern relative to the other contact structures, the pattern comprising an alternating distribution of other contacts and local resistor structures.

35. (Canceled)

36. (Canceled)

37. (Previously presented) The semiconductor device of claim 32, wherein current flow through the transistor is modulated by selective placement of a plurality of local resistor structures above the emitter.

38. (Original) The semiconductor device of claim 37 further comprising a plurality of contacts above the emitter, wherein a plurality of local resistor structures are formed, each within each of a group of the plurality of contacts in an interdigitated pattern, the pattern comprising an alternating distribution of contacts and local resistor structures.

39. (Currently amended) A semiconductor device integrating a local resistor element having a resistance value of from about one Ohm to about 100 Ohms, comprising:

an interlevel dielectric substrate;

a gate structure formed within the substrate having a source implant region and a drain implant region;

a contact formed within one of the source implant region and the drain implant region;

a first thin resistor film deposited on the contact;

a refractory metal film deposited on the thin resistor film; and

a conductive metal deposited on the refractory metal film;

wherein the contact, the first thin resistor film, the refractory metal film and the conductive metal define the local ~~resister~~ resistor element.

40. (Original) The semiconductor device of claim 39, further comprising a dopant implanted into said thin film.

41. (Currently amended) The method of claim 3, wherein the thin resistive ~~material~~ film layer is ~~a thin film~~ chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

42. (Currently amended) The method of claim 41, wherein the thin resistive ~~material~~ film layer is about 35 Angstroms thick and has a resistance value of no more than around 50 Ohms.

43. (Currently amended) The method of claim 41, wherein the thin resistive film ~~material~~ layer is about 50 Angstroms thick and has a resistance value of between about 100 Ohms to about 500 Ohms.

44. (Currently amended) The method of claim 41, wherein the thin resistive film ~~material~~ layer is about 200 Angstroms thick.

45. (Previously presented) The method of claim 4, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

46. (Previously presented) The method of claim 7, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

47. (Previously presented) The method of claim 12, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

48. (Previously presented) The method of claim 47, wherein the resistive material layer is about 35 Angstroms thick and has a resistance value of no more than around 50 Ohms.

49. (Previously presented) The method of claim 47, wherein the resistive material layer is about 50 Angstroms thick and has a resistance value of between about 100 Ohms to about 500 Ohms.

50. (Previously presented) The method of claim 47, wherein the resistive material layer is about 200 Angstroms thick.

51. (Previously presented) The method of claim 19, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

52. (Previously presented) The method of claim 51, wherein the resistive material layer is about 35 Angstroms thick and has a resistance value of no more than around 50 Ohms.

53. (Currently amended) The device of claim 23, wherein the thin resistive ~~material~~ film layer is ~~a thin film~~ chosen from the group consisting of a sputtered silicon

material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

54. (Currently amended) The device of claim 53, wherein the thin resistive ~~material~~ film layer is about 35 Angstroms thick and has a resistance value of no more than around 50 Ohms.

55. (Currently amended) The device of claim 53, wherein the thin resistive ~~material~~ film layer is about 50 Angstroms thick and has a resistance value of between about 100 Ohms to about 500 Ohms.

56. (Currently amended) The device of claim 53, wherein the thin resistive ~~material~~ film layer is about 200 Angstroms thick.

57. (Previously presented) The device of claim 24, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

58. (Previously presented) The device of claim 27, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

59. (Previously presented) The device of claim 32, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

60. (Previously presented) The device of claim 59, wherein the resistive material layer is about 35 Angstroms thick and has a resistance value of no more than around 50 Ohms.

61. (Previously presented) The device of claim 59, wherein the resistive material layer is about 50 Angstroms thick and has a resistance value of between about 100 Ohms to about 500 Ohms.

62. (Previously presented) The device of claim 59, wherein the resistive material layer is about 200 Angstroms thick.

63. (Previously presented) The device of claim 39, wherein the resistive material layer is a thin film chosen from the group consisting of a sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, and an amorphous polysilicon.

64. (Previously presented) The device of claim 63, wherein the resistive material layer is about 35 Angstroms thick and has a resistance value of no more than around 50 Ohms.